SHMAC: An Infrastructure for Heterogeneous Computing Systems Research

Thematic session on Evaluation of Heterogeneous Systems and their Applications
HiPEAC Computing Systems Week, Tallinn

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EECS Technical Motivation

Energy efficiency is becoming the primary design goal across all market segments

Extremely energy sensitive systems

- Lifetime of system is equal to battery life
- Lower energy consumption can open new markets

Mobile systems

- Energy: Users want long battery life
- Limited size of cooling system results in strict power constraints

Desktop computers

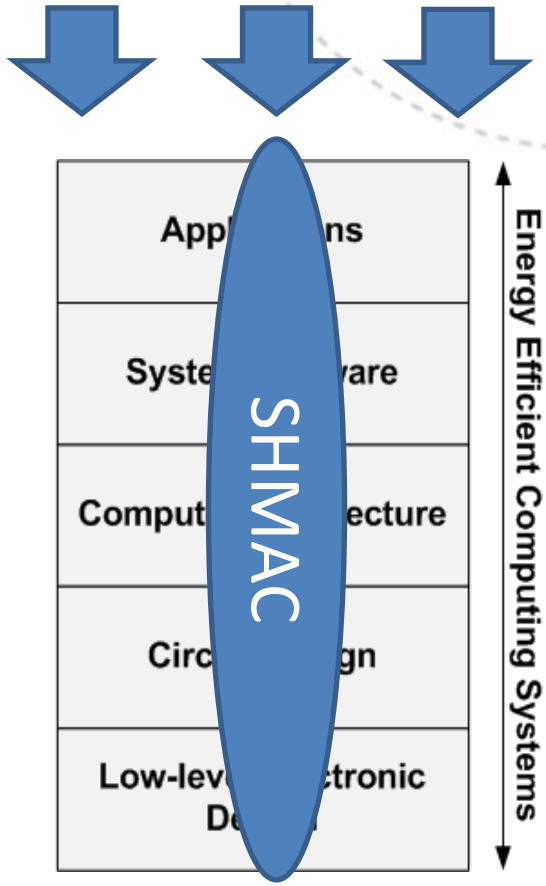
- Fixed power budget due to cooling challenges
- Cannot improve performance without improving energy efficiency

Data centers and HPC

- Energy bill dominates operating cost
- Power consumption is a significant engineering challenge

EECS Structure

- Vertical approach
  - Leverage strong groups working horizontally
- Application agnostic
  - Matches focus of high-volume international industry
  - Choose demonstrator applications that clearly demonstrates proposed innovations
- People
  - 6.2 affiliated permanent staff
  - 10 affiliated PhD students
  - 5 affiliated researchers/lecturers



Business as usual?

Business-as-usual scenario:
Add more cores and increase clock frequency

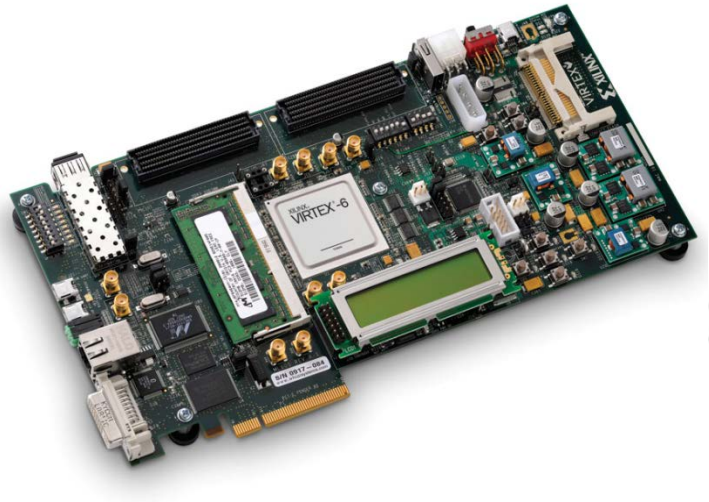
Practical server limit (about 100W)

Practical desktop limit (about 65W)

Paradigm shift from area- to energy-constrained computing

Result: Heterogeneous computing platforms

The SHMAC Project

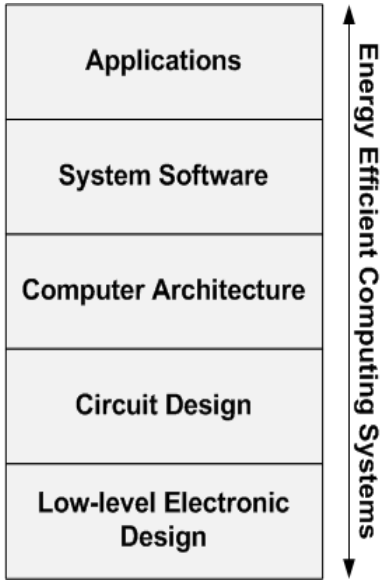


Dark silicon effect makes heterogeneous processors likely

Software for heterogeneous processors is an open research problem

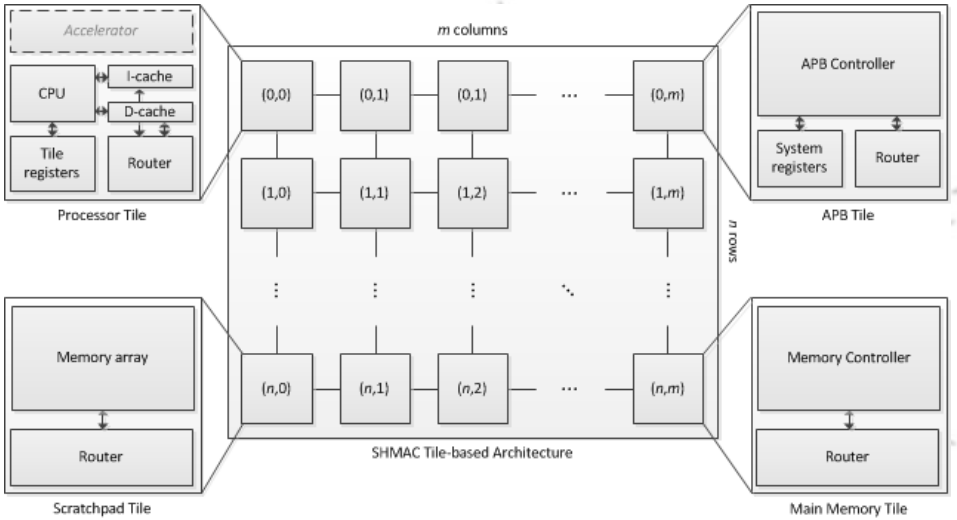
- Heterogeneity of off-the-shelf components is limited
- Simulators have unlimited heterogeneity but are slow

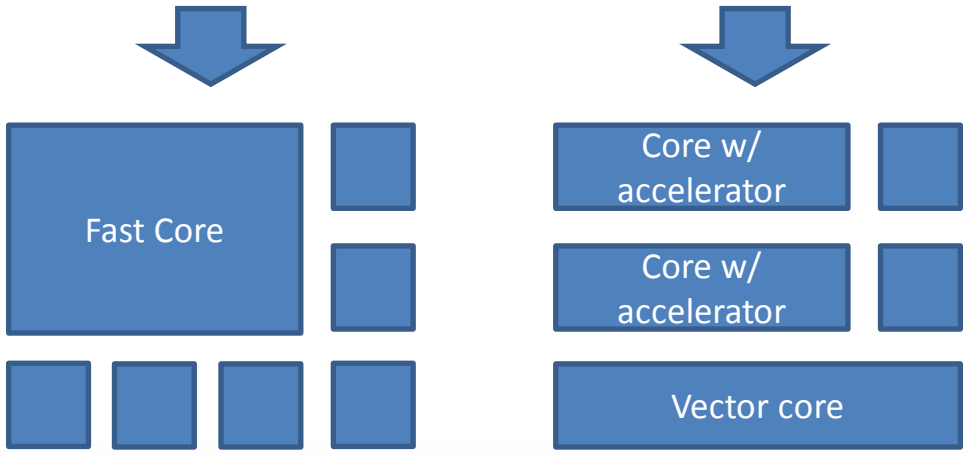
Solution: SHMAC = Single-ISA Heterogeneous MAny-core Computer



SHMAC Architecture

- Tiled multi-core design paradigm describing a class of processor architectures
- Common instruction set and architecture model gives software portability across SHMAC instances
- SHMAC instances can contain various tile types:
  - Processors with different energy/performance characteristics
  - Optimized processors (vector, OOO, etc.)
  - Accelerators





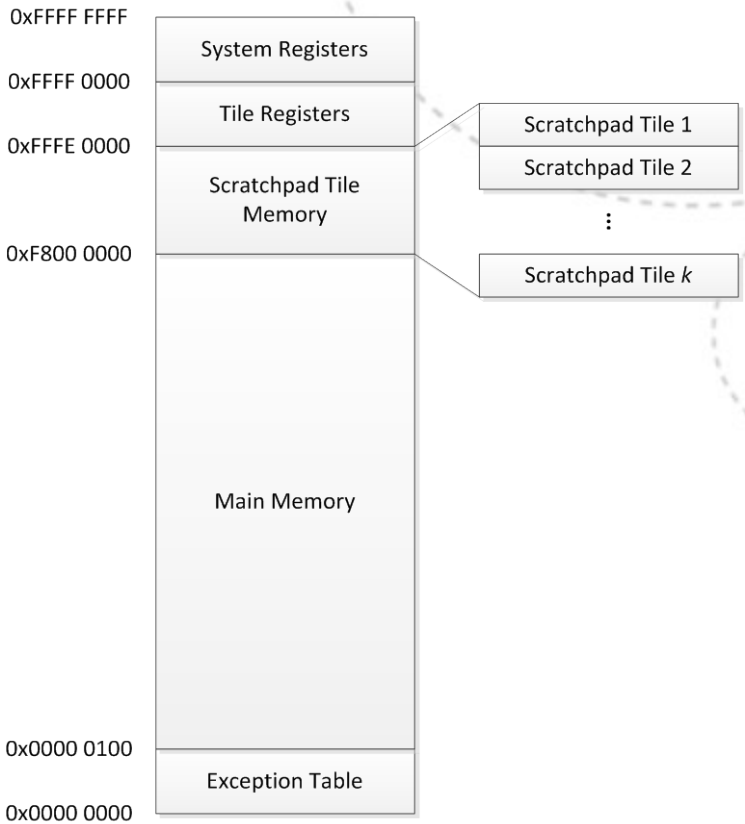
Design Goal: Software Portability

All processor tiles are functionally equivalent

- Performance may be very different
- Different processor classes and accelerators

Uniform architecture

- All processing tiles see the same memory map
- Tile registers are per-tile, other memory locations are global



SHMAC Memory Map

Research question: What are the costs associated with the Single-ISA abstraction?

Leveraging Reconfigurability

Generic components

- In-order core
- Core w/ accelerator
- Vector core
- Scratchpad

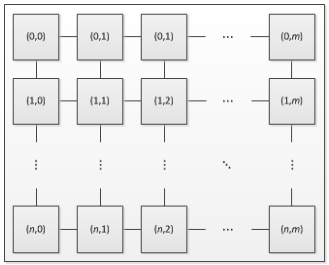
Synthesis

SHMAC Configuration

Benchmarks

Operating Systems

Runtime Systems



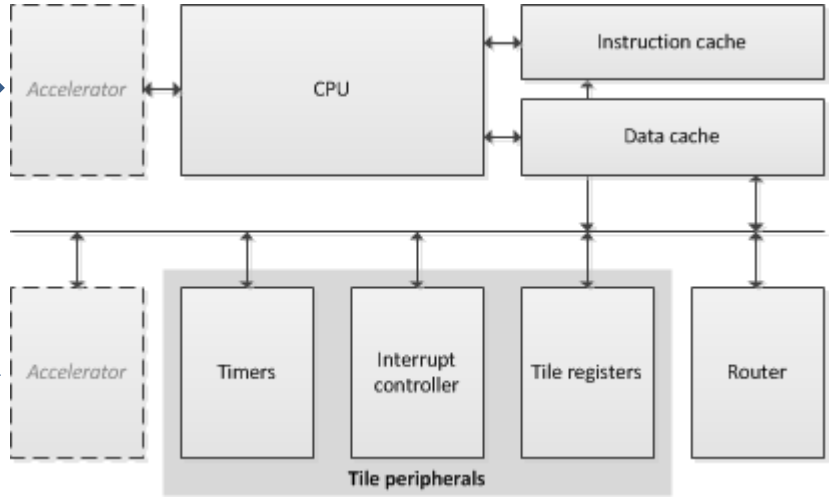
SHMAC instance running on an FPGA

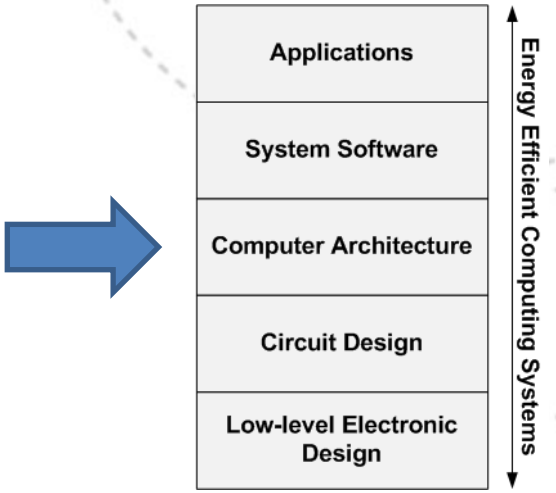
Measure, evaluate, repeat

Project Example 1: Integrating Accelerators

Tightly-coupled accelerator

Loosely-coupled accelerator





Accelerator research topics:

- Tightly vs. loosely coupled accelerators
- Which accelerators should be included?
- How can accelerators be leveraged by programmers?

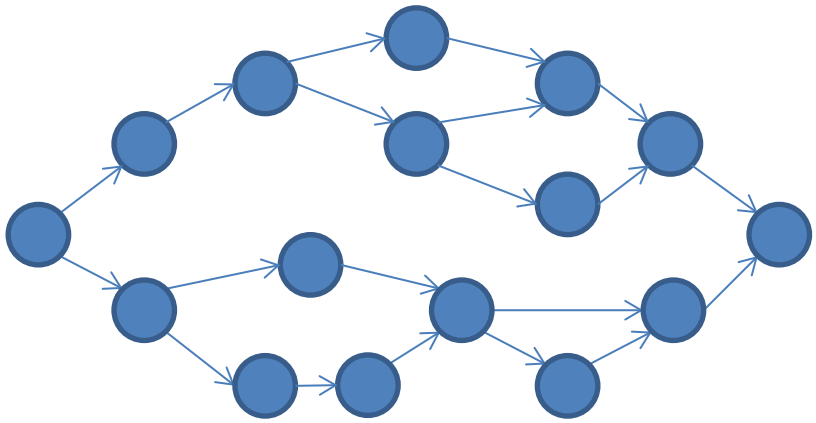
The most efficient solution will most likely require both software and hardware changes

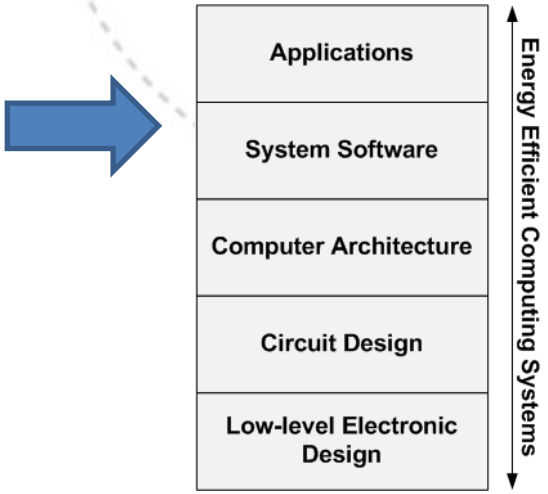
Key SHMAC Components:

- Accelerator support
- Processor tiles
- Memory tiles
- System Software
- Benchmarks

Project Example 2: Task Based Parallelism (TBP) for Heterogeneous Systems

TBP:
Program is organized as DAG of tasks (nodes) and dependencies (edges)





Task scheduling for energy efficiency :

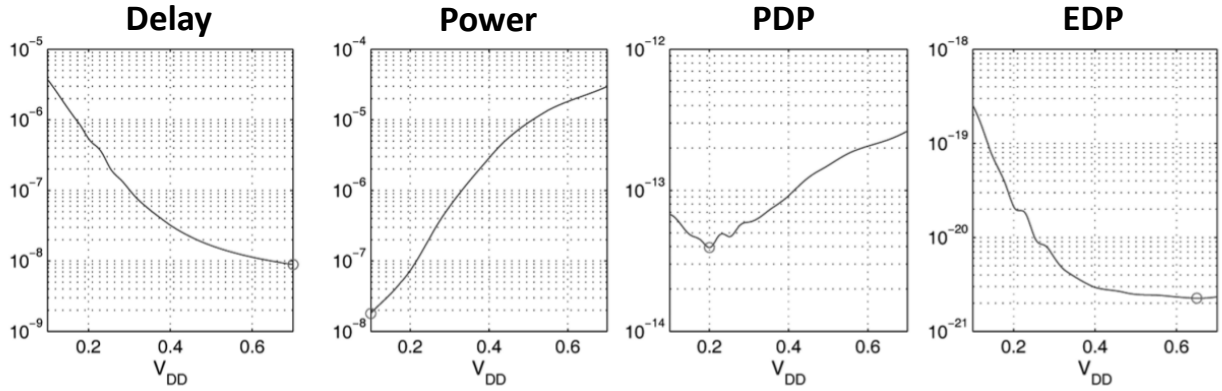
- How should tasks be scheduled in a heterogeneous environment?
- Which hardware feedback mechanisms are needed?

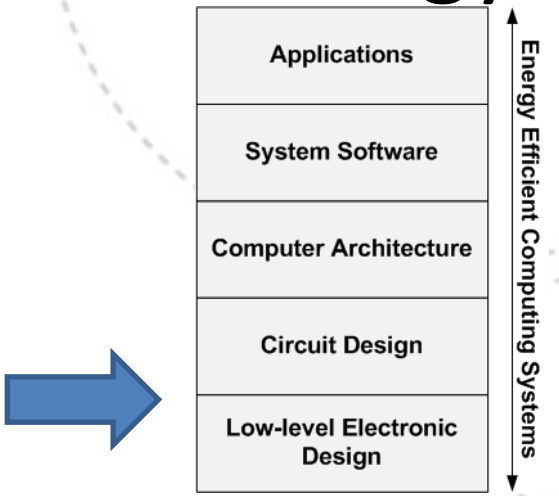
SHMAC advantages: Efficient software development, large diversity in systems, possibility to add feedback components

Key SHMAC Components:

- OS support
- Benchmarks
- Processor tiles
- Memory tiles

Project Example 3: Exploiting Near-/Sub-threshold technology



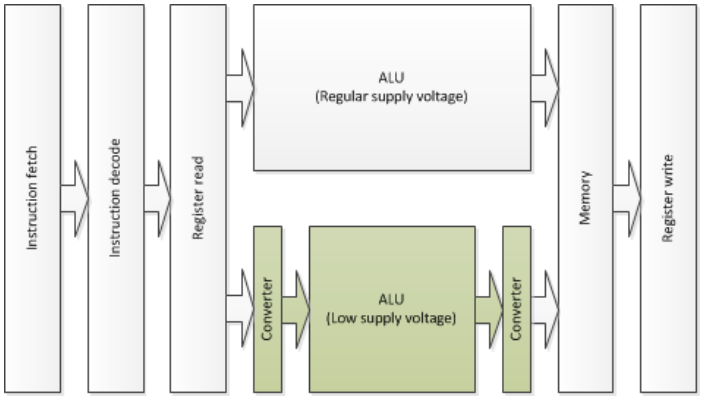


Reducing the supply voltage to near the threshold gives:

- Energy per switching is reduced by one order of magnitude
- Latency increases by 3-4 orders of magnitude

How can this technology be leveraged at the microarchitecture level?

Tape-out necessary to validate implementation



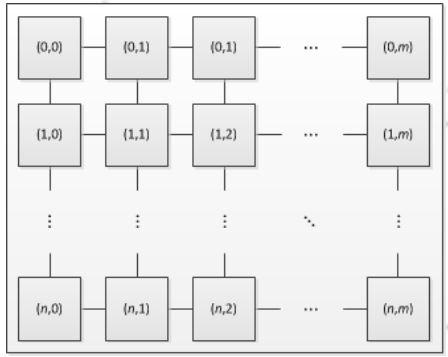
Key SHMAC Components:

- Processor tiles
- System Software
- Benchmarks

SHMAC Enables Collaboration

SHMAC combines generic components and powerful abstractions

- Reimplement/extend the part(s) involved in your research project



SHMAC best suited for cross-disciplinary projects where hardware and software innovations are combined

- Different partners can focus on different parts of the system

EECS is one of seven groups at NTNU that receives special support towards Horizon 2020

Future Directions

Status: Minimal set of tiles to support software development

Future hardware

- Efficient accelerator integration
- Vector core
- Out-of-order core

Future software

- Benchmarks (micro, macro)
- Operating Systems (conventional, multikernel)
- Runtime systems

Significant effort: 1 Post doc., 2 PhD students, 15 master students

Concluding Remarks

SHMAC Project

- An infrastructure for heterogeneous systems research
- Potential tool for a large variety of research projects
- Significant effort at NTNU

External Funding

- Strong relations to international high-volume industry
- Ambitious strategy for securing external research funding

Thank You!

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