Flexibility of generator and converter

Efficiency comparison between two-level and multi-level converter

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HydroFlex

Increasing the value of hydropower through increased flexibility

Deliverable 4.6 Efficiency comparison between two-level and multi-level converter

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Executive Summary

This report presents the work that was partially done under Task 4.3 of *WP4-Flexibility of generator and converter* and covers entirely the Deliverable 4.6, which aims at comparing the efficiency of the two-level converter with multi-level converters.

The target of the HydroFlex project is to increase the value of hydropower through increased flexibility, and variable speed operation is preferred for achieving that target. One of the important components for the variable speed operation is the power electronic converter, which is between the hydro generator and the gird. To cope with the fluctuations of the energy production brought by the renewable energy source, a large number of start-stops are required in the daily operation of the pumped storage hydropower unit. These cyclic start-stops imposes thermal stress on the converter; thus, it is important to choose the right converter topology for such applications.

In this deliverable, the losses of the two-level converter and different multi-level converter topologies are compared. Different modulation techniques and control strategies for different targets are implemented in this deliverable as well. MATLAB Simulink and PLECS are the tools used in this study to simulate the electrical and thermal behaviour of the converter.

It is found that the nine-level MMC converter has the lowest losses for the defined boundary conditions of the application. For 100% power delivery of the nine-level MMC system, the value of the loss is 0.63% of the nominal power. The five-level NPC has the second lowest losses, which is 0.68% of the nominal power under 100% power delivery. However, the complicated control and uneven temperature distribution of the NPC topology make it less attractive. The five-level MMC could be a good alternative compared to the five-level NPC, if the switching losses could be further minimized. The losses of different converters have the same pattern for the other power levels.

Apart from the loss evaluation of the converter, the junction temperature of the power switches inside the converter are evaluated as well. The junction temperature profile can be used to estimate the lifetime of the power switches, though the usage of a lifetime model is needed.

The last part of the report is the experiment results of a five-level MMC. The experiments are compared with simulation, and the waveforms from the experiments verify the feasibility of the modulation and control methods for the MMC converter.

This report contains the following sections:

Section 1 is the introduction of the report.

Section 2 discusses the modelling process. To evaluate the efficiency and losses of the converter, both the electrical modelling and thermal modelling of the converter need to be done. In this report, a detailed process of the loss evaluation is presented.

Section 3 presents the simulation results. The analysis regarding the current THD, the components count, the losses of the converter and the junction temperature of the power switches inside the converter are discussed.

Section 4 presents the experiment results of the five-level MMC with different modulation techniques and control methods.

Section 5 presents the conclusion of this report.

Table of Contents

Abbreviations

AC	Alternative current
ANPC	Active neutral-point-clamped
DC	Direct current
FEM	Finite element method
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
MMC	Modular multilevel converter
MV	Medium voltage
NPC	Neutral-point-clamped
PWM	Pulse width modulation
SPWM	Sinusoidal pulse width modulation
SVM	Space vector modulation
THD	Total harmonic distortion

1 Introduction

Renewable energy, such as wind power and solar power, plays an important role in reducing the greenhouse emissions. Unfortunately, renewable energy also brings fluctuations to the energy generation due to their intrinsic characteristics. Therefore, to facilitate the integration of renewable energy into the grid, flexible energy storage methods are needed. One of the solutions for the energy storage is to employ the century-old pumped storage hydropower technology. Traditionally, under generation mode, pumped storage hydropower operates with fixed speed; however, it is found that variable speed operation can bring several advantages to the system over fixed speed operation [1], and one of the important advantages of variable speed operation is the higher overall efficiency of the system [2][3].

To achieve variable speed operation, a power electronic converter is needed as the key interface between the hydro generator and the grid. In this deliverable, a synchronous generator/motor along with a full-size converter are modelled. When frequent start-stops occur in the daily operation of the pumped-storage hydropower plant, it is important to have a converter with high efficiency. High efficiency means less loss, and that means more profit can be earned from the system.

One of the most common used converter topology in industry applications is the two-level converter. However, for the medium voltage (MV) application, in which the nominal system voltages are greater than 1 kV and less than 100 kV [4], it is a challenge to use the two-level converter due to the constraints of voltage and current ability of the power electronics. Besides, the current and voltage total harmonic distortions (THDs) are quite high in the two-level converter system, which means increased cost for additional filters in the set-up. Therefore, the multi-level converter is preferable in such MV applications.

In this deliverable, the studied multi-level topologies are the neutral-point-clamped (NPC) converter topology and the modular multi-level converter (MMC) topology. The three-level NPC converter that was introduced in [5] in year 1981, and since then, it has been started to be applied in high-power medium voltage applications [6]. Apart from the three-level NPC, the five-level NPC is also studied in this deliverable. The modular multilevel converter (MMC) topology which was introduced in [7] has been successfully applied in voltage source converter high-voltage direct current (VSC–HVDC) transmission systems, and now it is being used in variable speed drive as well [6]. In this deliverable, the five-level and nine-level MMC are studied.

The following sections of the report contains these parts: the process of modelling and control of the converter; the efficiency comparison results between different converters; the experiment results of a five-level MMC; and the conclusion.

2 Converter modelling

The overall process of the converter modelling is shown in Fig. 1, and it contains three different layers. The first layer is MATLAB Simulink, and the system controllers and converter modulation strategies are implemented in this layer. The second layer is PLECS electrical simulation domain, the converter electrical model is built in this layer, and the electrical behaviour of the converter is being simulated. The third layer is also in PLECS, but it is in the thermal domain. The power electronics junction temperature, the switching loss and the conduction loss of the converter are being modelled in this layer. The detailed process of electrical modelling and thermal modelling are being described in the following parts.

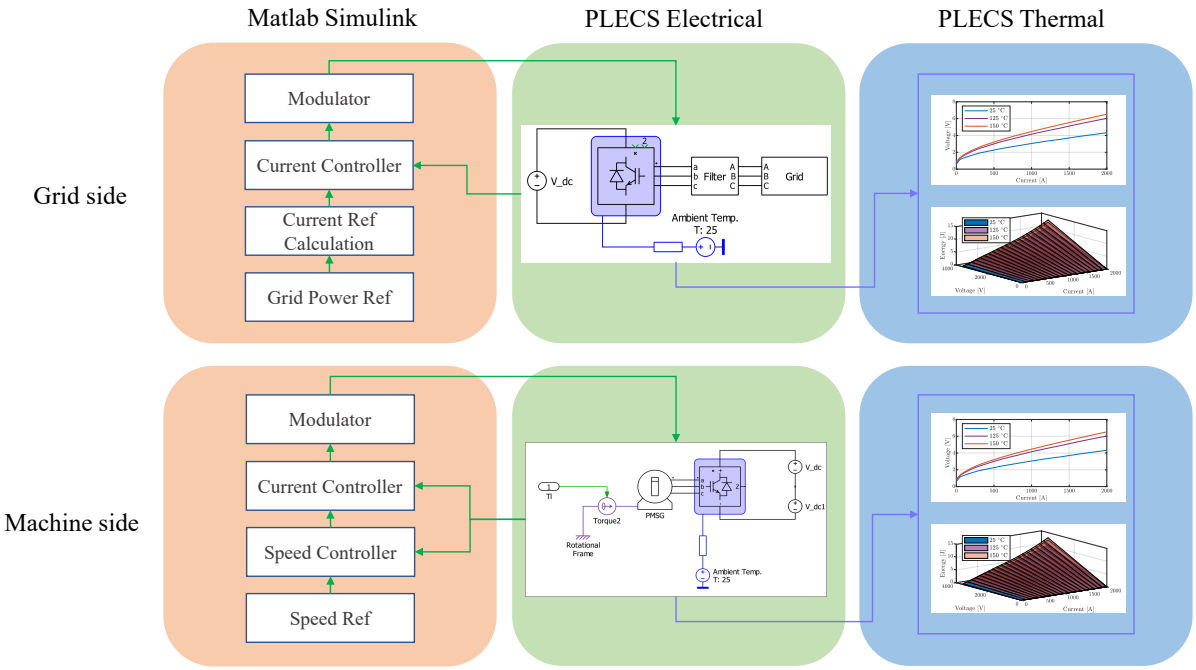


Fig. 1: The process to evaluate the losses inside the converter

2.1 Electrical modelling

2.1.1 Two-level converter

The electrical model of the two-level converter is shown in Fig. 2. It should be mentioned that for each switch position in the two-level converter, several power semiconductors may be connected in series and parallel to meet the power and current requirements of the system. For example, if the DC-link voltage is 13 kV, and the blocking voltage of used power semiconductors is 3.3 kV, then, the switch S_1 in Fig. 2 needs 8 of these power semiconductors being connected in series to withstand the blocking voltage.

Both the pulse width modulation (PWM) and space vector modulation (SVM) can be used for generating the gate signals of the two-level converter.

2.1.2 NPC converter

The schematic diagrams of a three-level NPC converter with using clamping diodes is showing in Fig. 3, and the diagram of one phase leg of a five-level NPC converter is shown in Fig. 4. It can be seen that The structure of the five-level diode clamped NPC is similar to the three-level converter, apart from two more common DC-link capacitors and more power semiconductors. The same as for the two-level converter,

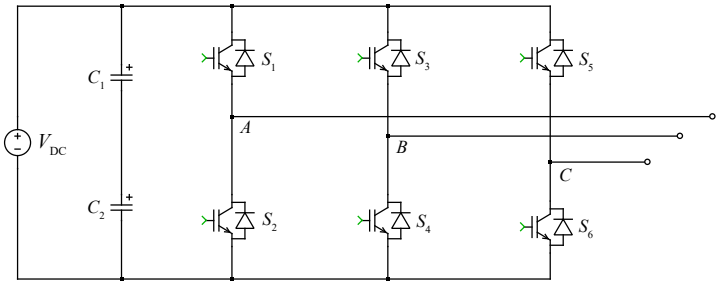


Fig. 2: Schematic diagram of a two-level converter

both PWM and SVM modulations can be used for generating the gate signals of the power switches in the NPC converter.

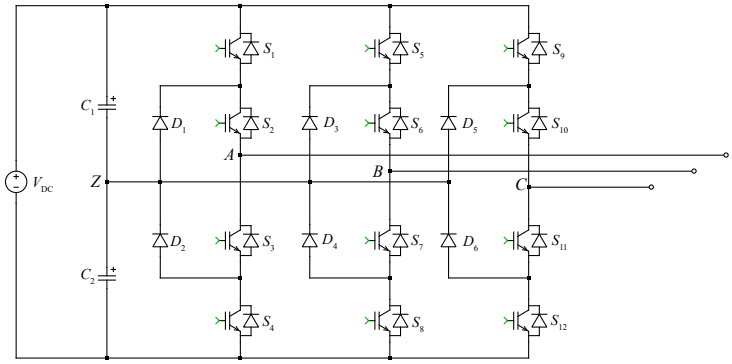


Fig. 3: Schematic diagram of a three-level NPC converter

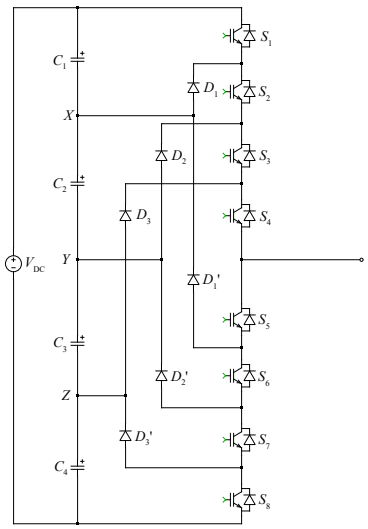


Fig. 4: Schematic diagram of a three-level NPC converter

Taking the three-level NPC as an example, the switching states and the operating states of it for one phase are shown in Table I.

Same as the two-level converter, both PWM and SVM modulations can be used for generating the gate signals of the power switches in the NPC converter.

Table I: Switching states and terminal voltage of a three-level NPC

Switching State	Device Switching States (Phase A)				Terminal Voltage (v_{AZ})
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	$V_{DC}/2$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-V_{DC}/2$

2.1.3 Neutral point voltage deviation

One of the issues for the NPC converter is the neutral point voltage deviation in the common DC link. As shown in Fig. 3, the potential of the neutral point Z increases when the current flows into it and vice versa. This can be more intuitively illustrated as in Fig. 5, when the three-phase switching state of the converter is POO, which means phase A is connected to positive DC-link voltage and phase B and C are connected to the neutral point of Z, the current will flow into Z, thus, increasing the potential of the neutral point. For switching state NOO, similar analysis can be applied, and the current will flow out of the neutral point, making the neutral point potential decrease.

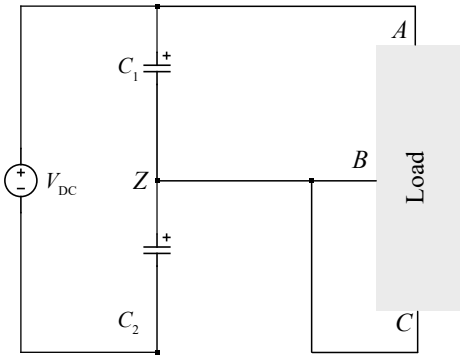


Fig. 5: Neutral point potential increase due to flow-in current under POO state

To sum up, for a three-level NPC,

- Zero vectors, PPP, OOO and NNN, do not affect the neutral point voltage v_Z;
- Small vectors, for example POO, have a dominant influence on v_Z;
- Medium vectors, for example PON, can affect v_Z, but the direction of voltage deviation is undefined.
- Large vectors, for example PNN, do not affect v_Z.

For the five-level NPC in Fig. 4, the neutral points of X, Y and Z face a similar issue of voltage deviation.

Some other aspects, such as unbalanced three-phase operation, unbalanced DC capacitors due to manufacturing, inconsistency in the switching device can cause the deviation of neutral point voltage as well.

To deal with the neutral point voltage deviation, different methods have been developed based on different modulations. For PWM based modulation, the common method is to inject a zero sequence signal in the modulation signal to compensate for the deviation of v_Z. For SVM based modulation, the small vectors and medium vectors of redundant switching states are used to balance v_Z. For the five-level NPC converter, the method is more complicated, due to the complicated structure of the converter.

Fig. 6 shows the general solutions in NPC converters that can be used to balance the neutral point voltage [8]. The solutions can be divided into two categories, software-based solution and hardware-based solution. For the software-based solution, by using open loop or closed loop control, the modulation signal is being modified, thus, the neutral point voltage is balanced. For the hardware-based solution, usually back-to-back configuration is needed [9], or additional external circuits which work as independent DC-DC converter are needed in the DC-link.

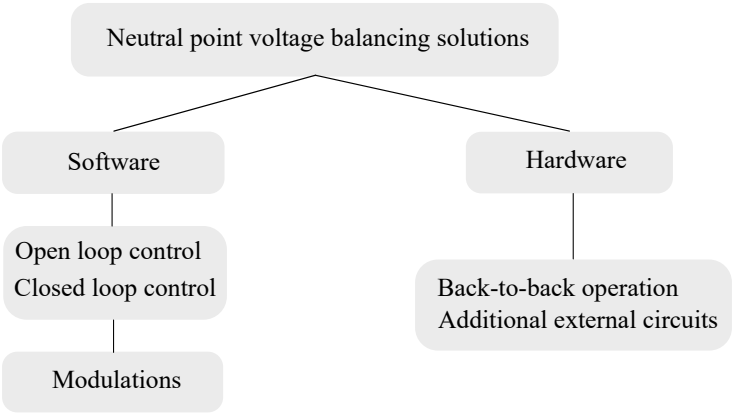


Fig. 6: Solutions for neutral point voltage balancing in NPC converters

2.1.4 Uneven temperature distribution of NPC

Another issue with the NPC converter is the uneven temperature distribution among the power semiconductors. Fig. 7 shows the temperature inside the switches in the upper arm of phase A of the three-level NPC, and it can be seen that the IGBT of the outer switch S_1 has the highest temperature while the diode of the inner switch S_2 has the lowest temperature. This uneven temperature distribution means that some switches inside the NPC converter will deteriorate faster than the other switches.

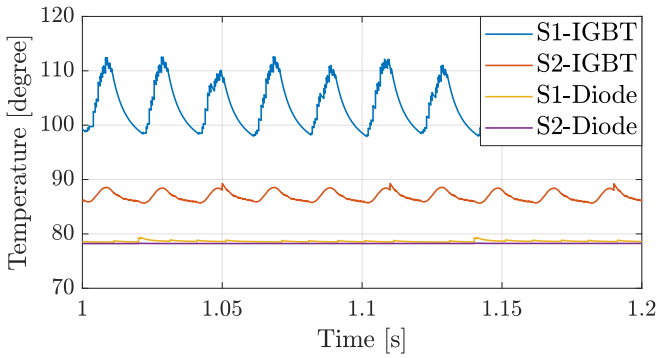


Fig. 7: Temperature inside the power semiconductors of the NPC converter

To deal with this issue, the active NPC (ANPC) converter is developed [10]. By using active power switches to clamp the neutral point, losses of the switches can be redistributed, and the temperature will be more evenly arranged among the power switches [6]. However, for the high level ANPC converter, the modulation gets complicated, while the uneven temperature distribution among the switches is not greatly improved. Furthermore, some of the control methods of the ANPC converter can increase the total loss of the converter.

2.1.5 MMC converter

As described in the introduction part, the other topology of multi-level converter is the MMC topology, and the schematic diagram of the MMC is shown in Fig. 8 [7]. Each arm of the MMC consists of n number of submodule (SM) and one arm inductance. The SM used in this study is a half-bridge IGBT submodule. The other submodules, like the full-bridge submodule or three-level submodule can be used in the MMC as well.

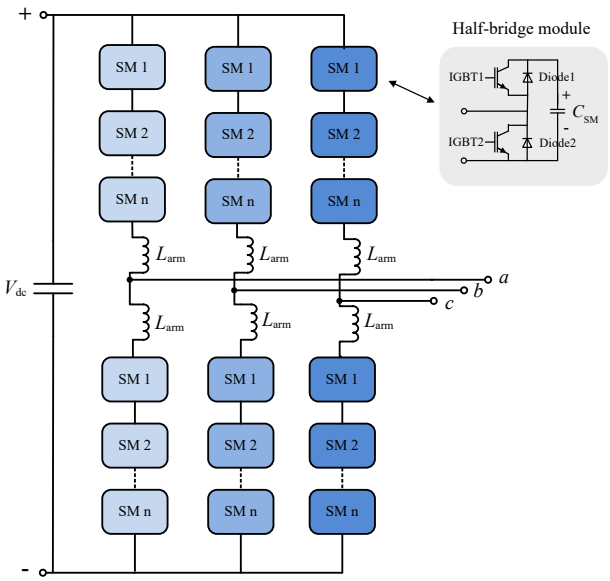


Fig. 8: Schematic diagram of the MMC topology

The same as for the two-level converter and the NPC converter, the MMC can employ PWM and SVM to generate the gate signals for the converter.

2.1.6 Circulating currents

One of the challenges in the MMC modelling is the control of the circulating currents of the MMC. It has been proved that the circulating currents in the MMC are generated by the inner voltage difference for each phase and the common DC-link, and they are in the form of negative sequence with the frequency of twice the fundamental frequency. In this deliverable, the method of suppressing the circulating current is called double line frequency circulating current controller [11].

In Fig. 9a, the arm currents and the circulating currents of phase A in a MMC converter are shown to illustrate the effect of the circulating current controller. At time of 0.3 s, the circulating current controller is activated and the amplitude of the circulating current is greatly reduced from around 280 A to 110 A. The reduce of circulating currents reduces the conduction loss inside the MMC.

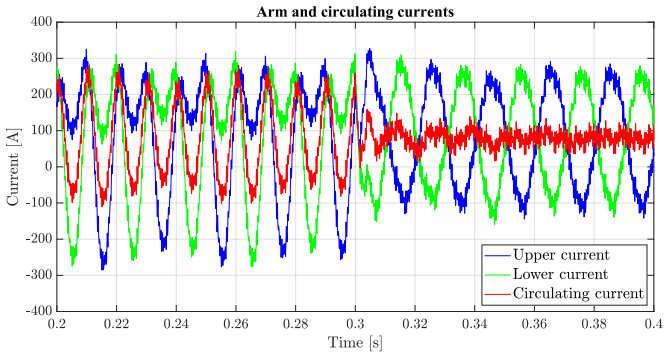
2.1.7 Capacitor voltages in submodule

The other challenge in the MMC modelling is the unbalanced capacitor voltage in each SM. To balance the voltage inside the submodule of the MMC, a sorting and balancing algorithm, which is based on the submodule capacitors voltage comparison and the polarity of the arm currents, is employed at the modulation stage [12].

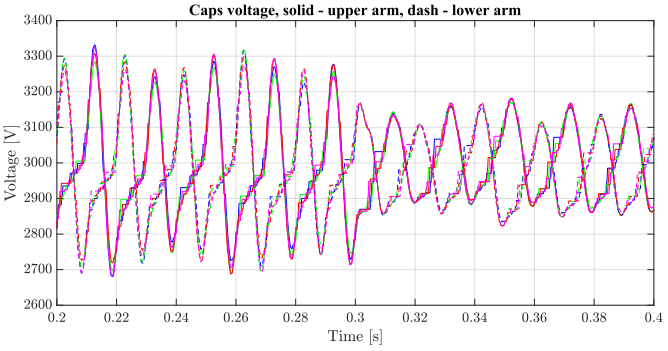
Apart from the unbalanced voltage in the MMC submodule, another issue is the voltage ripple in each SM, a limitation of the voltage in the SM impacts in the size of the capacitor in each SM. It is found

that the voltage ripple is dominated by the fundamental and second-harmonic components, and with the circulating currents suppressed, the voltage ripple can be decreased as well [13].

Fig. 9b presents the voltage of each SM in a MMC when the sorting and balancing algorithm is employed, and the circulating current controller activates at time of 0.3 s. It can be seen that the SM capacitor voltages are balanced before time of 0.3 s, and once the circulating current controller is activated, the voltage ripple is reduced as well.



(a) Circulating currents in phase A of a MMC

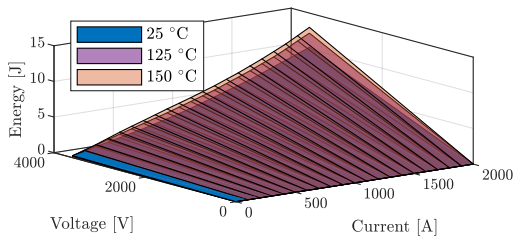


(b) Submodule voltages in phase A of a MMC with balancing and sorting method

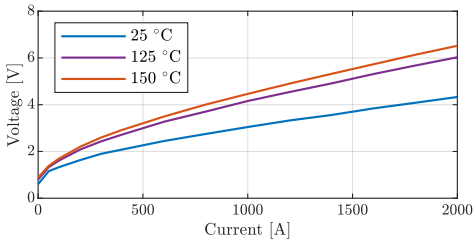
Fig. 9: Circulating currents and SM capacitor voltages in a MMC

2.2 Thermal modelling

The first part of thermal modeling is to calculate the losses of the power switches. One way to calculate the losses is using the loss lookup tables in PLECS thermal simulation, and an example of the IGBT turn-on loss and conduction loss lookup tables are shown in Fig. 10.



(a) IGBT turn-on loss lookup table



(b) IGBT conduction loss lookup table

Fig. 10: IGBT turn-on and conduction losses lookup table example in PLECS

The second part of the thermal modeling is to calculate the junction temperature in the power switches.

Once the losses in the power switches are acquired for different operating points, the junction temperature of the power switches T_j can be evaluated by the equivalent thermal network in Fig. 11. It should be mentioned that the loss and junction temperature evaluation is an iterative procedure, since the junction temperature impacts back on the losses, and so forth, so a number of iterations are needed to find the steady-state loss and junction temperature values.

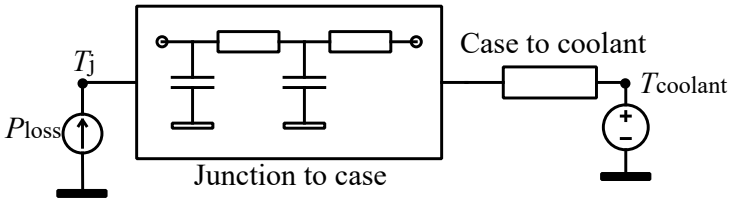


Fig. 11: Equivalent thermal network from junction to coolant

The parameters of the junction to case thermal network are often given in the datasheet of the power switches, while the information of the case to coolant thermal impedance is usually missing. In order to get the thermal impedance from case to coolant, a finite element method (FEM) model of the power switch together with the heatsink is built in COMSOL. Fig. 12 shows the 3D model of the IGBT power module with a heatsink in COMSOL.

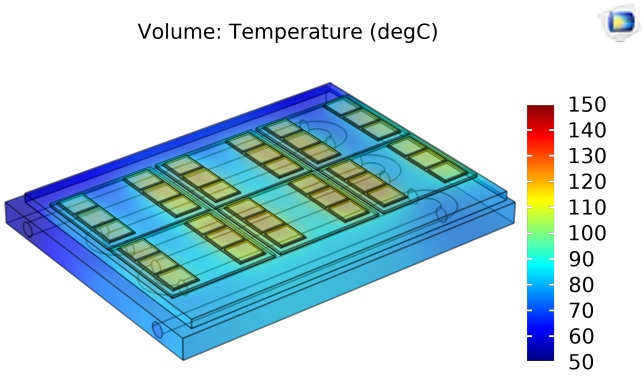


Fig. 12: COMSOL 3D simulation model of the IGBT power module

The thermal impedance Z_{th} from the case of the power module to the coolant is determined from the COMSOL simulation result, and it is 0.01 K/kW with the designed heatsink in Fig. 12.

2.2.1 Lifetime modeling

Using the results from the thermal modelling, the lifetime of the power switches inside the converter can be estimated. Once the losses of power switches inside the converter are acquired, with using the thermal model in Fig. 11, the junction temperature of the power switches can be acquired as well. Then, the lifetime estimation can be done based on the power switches junction temperature.

When evaluating the lifetime of the power switches, one important input is the mission profile. The mission profile defines the operating points of the system for a certain period, thus, the cyclic temperature swings of the power switches which are acquired when feeding the operating points into the previous thermal modeling steps. Fig. 13 shows the power deployment plan for a 21 MW hydropower unit from [14] with a data sampling rate of 15 mins, and this plan is the mission profile that defines all the operating points of the system for a one-year period.

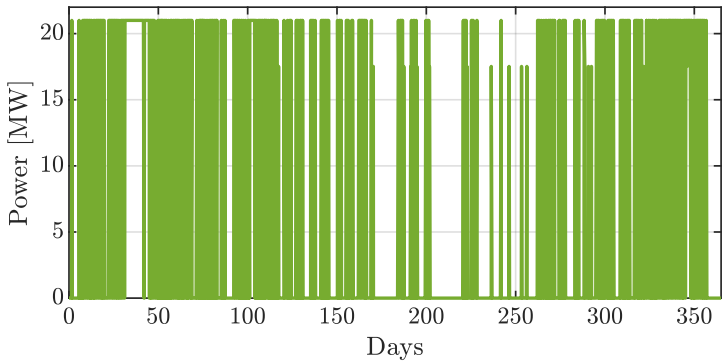


Fig. 13: Power dispatch plan of the studied hydropower unit

Apart from the mission profile, the lifetime model is another important part in the lifetime modelling. The lifetime model used in this study is introduced in [15], which is developed by Semikron, and is called the SKiM63 lifetime model [16]. This model isolates the degradation of different interconnections, and only the degradation of the wire bond connection to the chip determines the lifetime. It should be mentioned that in reality, the failure of the power switches contain other aspects, such as the chip solder degradation, etc. The life cycles, N_f, of the switches with respect to the temperature swing, ΔT_j, and the mean junction temperature, T_jm, is given by

$$\begin{aligned} N_f =& A \times (\Delta T_\mathrm{j})^{\alpha} \times (ar)^{\beta_1 \Delta T_\mathrm{j} + \beta_0} \times [\frac{C + (t_\mathrm{on})^{\gamma}}{C+1}] \\ & \times \exp(\frac{E_a}{k_b \times T_\mathrm{jm}}) \times f_\mathrm{diode} \end{aligned} \tag{1}$$

where the parameters are given in Table II.

Table II: lifetime model parameters

Parameter	**Value**	**Parameter**	**Value**
A	3.4368×10^{14}	α	-4.923
β_1	-9.012×10^{-3} 1/K	ar	0.31
β_0	1.942	C	1.434
E_a	6.606×10^{-2} eV	γ	-1.208
k_b	8.62×10^{-5} eV/K	f_diode	0.6204

The accumulated damage D of the switch for one repetition of the mission profile can be determined by Miner's rule,

$$D = \sum_{i=1}^{n} \frac{N_i}{N_{fi}} \tag{2}$$

where N_i can be acquired from the rainflow counting algorithm [17] and N_{fi} can be calculated from (1). The inverse of D times the period time of the mission profile gives the lifetime of the power switches.

3 Simulation results

3.1 Boundary conditions for loss evaluation

To evaluate the losses inside different converter topologies, the boundary conditions of the model are listed in Table III, and the simulation focus on the grid-side converter.

Table III: Simulation model parameters

Parameters	Value	Unit
Power S	6	MVA
Power factor φ	1	/
DC-link voltage V_{DC}	13	kV
Grid phase peak voltage $V_{g,peak}$	5.5	kV
Grid frequency f	50	Hz
PWM frequency modulation ratio m_f	23	/
RL filter Resistance R_f	20	mF
RL filter inductance L_f	26.8	mΩ

From the power and voltage in the boundary conditions, it can be seen that the RMS current in one phase is around 500 A, and the 5SNA-1000G650300 and the 5SNA-1000N330300 from Hitachi Energy are selected as the power switches to get the converter losses in the simulation model. Both of the switches have the ability to handle a maximum current of 1000 A.

3.2 Current THD

The first part of the simulation results presented in Fig. 14 shows the THD of the current that is injected into the grid, and this indicates the size of the filter that needs to be utilized in order to have a good quality of waveform. The higher the THD, the larger filter is needed.

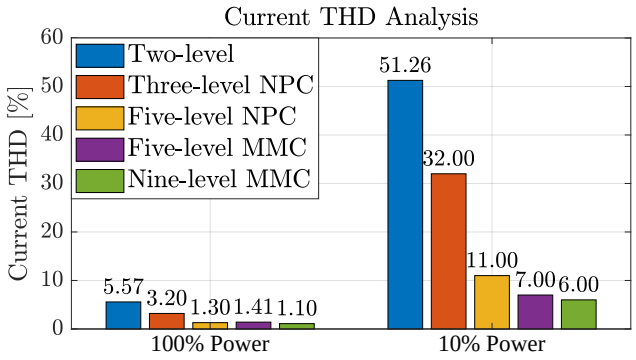


Fig. 14: Current THD of different converter configuration

It can be seen that due to the benefit of the high voltage levels in the converter, the nine-level MMC shows the lowest current THD both in 100% power and 10% power. For the two-level and three-level converter, the current THD is quite high, and this indicates that it is infeasible to apply these converters with the current system parameters.

3.3 Converter loss results

The second part of the simulation results is the converter loss, and the loss of the converter under different power levels are shown in Fig. 15. The nominal power of the system is 6 MVA, and all the loss values

in Fig. 15 are normalized with respect to the nominal power.

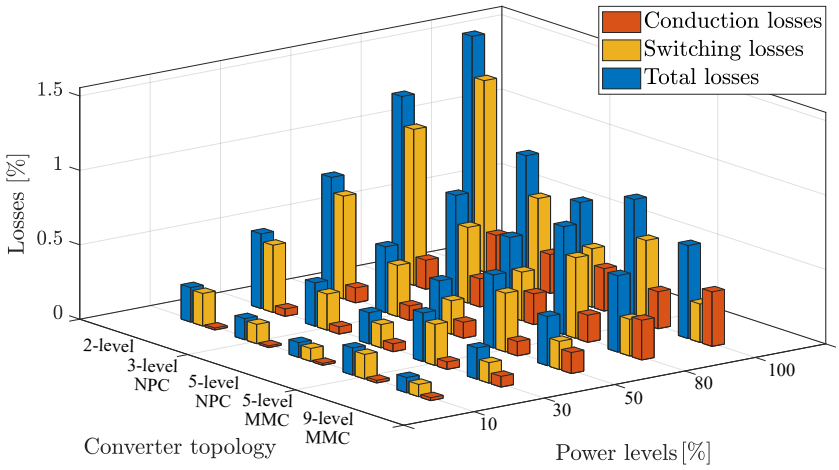
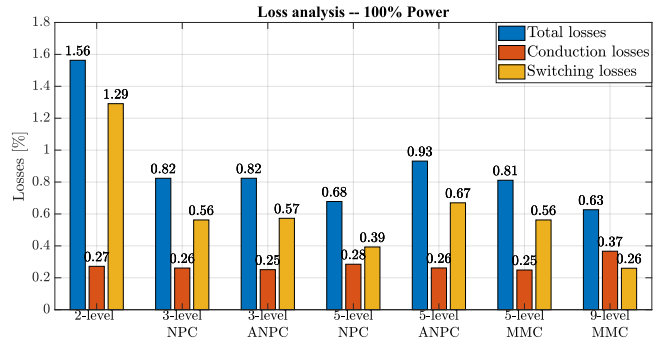


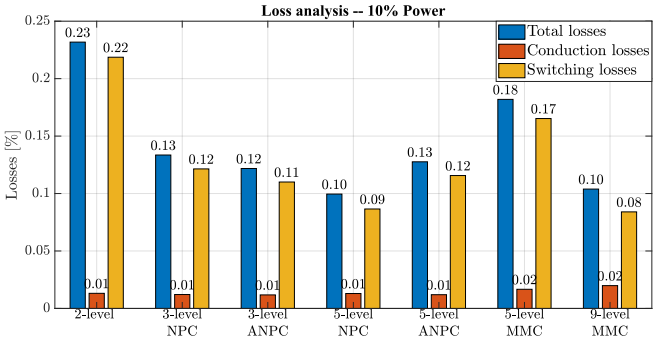
Fig. 15: Converter losses with various power levels

In general, it can be seen that the loss of the converter increases when the power level is increasing, and the two-level converter has the highest losses, while the 9-level MMC has the lowest losses. For the converters with less than five voltage levels, the switching loss accounts for the majority of the losses under different power levels. For the 9-level MMC, the conduction loss is higher than the switching loss under high power level.

In Fig. 16, the losses of the converter under 10% and 100% power are presented. In addition to adding the values of the losses on the figure, the losses of the ANPC converters are shown as well.



(a) Converter losses with 100% Power



(b) Converter losses with 10% Power

Fig. 16: Converter losses under 100% and 10% power level

Apart from the losses, the component count of different converter configuration is shown in Table IV.

Table IV: Components count of different converter configurations

Converter configuration	Components number count				IGBT power module type
	IGBT power module	Clamping diode	Independent capacitor	Independent inductor	
Two-level converter	24	/	/	/	5SNA-1000G650300
Three-level NPC	24	12	/	/	5SNA-1000G650300
Five-level NPC	24	36	/	/	5SNA-1000G650300
Five-level MMC	48	/	48	6	5SNA-1000G650300
Nine-level MMC	96	/	96	6	5SNA-1000N330300

Based on the above results, it is shown that of all the converter configurations, the nine-level MMC shows the lowest losses. However, the nine-level MMC needs the highest number of components, including 96 IGBT modules, 96 submodule capacitors, and 6 arm inductors for the defined boundary conditions. It should be mentioned that the nine-level MMC uses a smaller power switch 5SNA-1000N330300 compared with the other converter configurations. The price of 5SNA-1000N330300 is almost half of the other power switch 5SNA-1000G650300, thus the investment in the IGBT module in the nine-level MMC is almost the same when compared with the five-level MMC. Worth mentioning is that extra investment is needed for the driver circuits and submodule capacitors in the converter. This means that the total cost of the 9-level MMC would be the highest while the losses would be the lowest. Therefore, if the main target for designing the converter for the application is to have the lowest loss in the converter, the nine-level MMC would be the best option.

On the other hand, if the yearly power dispatch plan of the power unit is known, another analysis from the perspective of the total saved energy in one year can be conducted. Based on the mission profile for a 21 MW unit in Fig. 13, the mission profile for the simulated 6 MW unit can be derived by scaling down the power, and the calculated annual electricity generation of this 6 MW unit is around 14.8 GWh. According to the losses percentage values in Fig. 15, the annual converter energy losses of different converter topologies with the unit of [MWh] and [%] (with respect to the total annual energy production) are shown in Table V.

Table V: Annual converter energy losses of different converter topologies

Converter topology	Total losses [MWh]	Total losses [%]
2L	320.934	2.17
3L NPC	184.474	1.25
5L NPC	139.351	0.94
5L MMC	191.258	1.29
9L MMC	132.419	0.89

From Table V, it can be seen that the nine-level MMC has the lowest annual energy losses, and this matches with the previous analysis. The converter that generates the second lowest annual losses is the five-level NPC, and the loss difference between the nine-level MMC and the five-level NPC converter is 6.932 MWh. If the average price of 1 kWh electricity is 1 SEK, then the profit difference between the nine-level MMC and the five-level NPC converter would be 6932 SEK/year. Considering the power switch price, it can be estimated that it takes the nine-level MMC to be running for 98.5 years to accumulate the amount of money that is invested in the extra power switches compared with the five-level NPC. This 98.5 years can be decreased to some extent when considering the investment in the clamping power diodes in the five-level NPC converter. On the other hand, the reference mission profile in Fig. 13 shows that the power unit is not operating with full power all over the year, thus, this 98.5 years can be further decreased if the power unit is scheduled for delivering more annual energy.

If the target in the design of the converter is not only to maximize the efficiency of the converter but also to have the least complexity, then, the five-level NPC could be a good option for such an application. When using the same power switches, the five-level NPC shows the lowest losses inside the converter, and the total number of IGBT modules is only half of the five-level MMC. However, the five-level NPC needs some extra clamping diodes, and the neutral point voltage control and uneven distribution of the temperatures in different switch positions make the five-level NPC not that attractive.

The three-level NPC converter shows the third best performance among all the five converter topologies. However, when considering the extra investment on the clamping diodes and the external filter due to the higher voltage and current THDs, the five-level MMC can outperform the three-level NPC converter if the losses can be decreased. As shown in Fig. 16a, the switching loss is almost two times of that of the conduction loss in the five-level MMC at 100% power, thus, it is natural to think about how the switching losses can be decreased. One way of reducing the switching loss is to cut down the frequency of the sorting events for balancing the submodule capacitor in the MMC, while the voltage ripples in the MMC half-bridge modules will increase, which means a larger capacitor is needed for each of the submodules. Another way of decreasing the switching losses is to utilize the discontinuous SVM. By using the five-segment operation in the converter, the switching events in each PWM cycle can be decreased, thus lowering the switching loss.

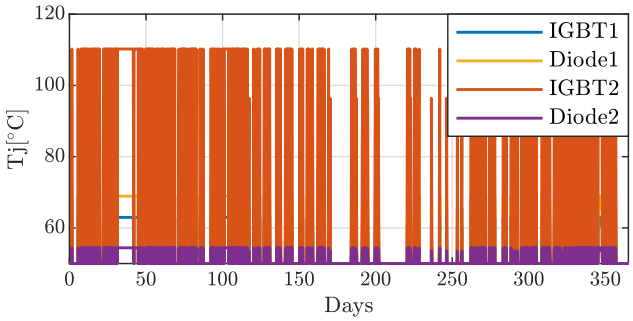
3.4 Power switches junction temperature estimation

The junction temperature estimation of the power switches inside a back-to-back MMC configuration is conducted with the converter parameters listed in Table VI.

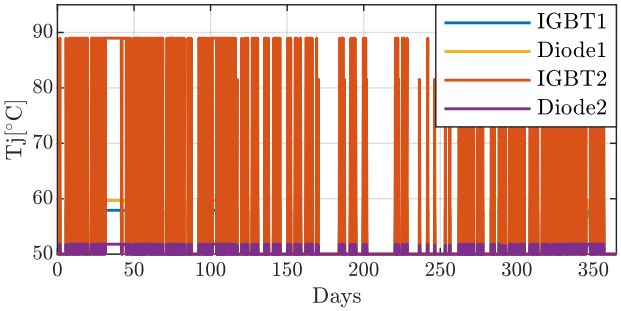
By feeding in the mission profile in Fig. 13, the junction temperature variations inside one half-bridge module of the MMCs are shown in Fig. 17. It can be seen that IGBT2 in the half-bridge module experiences the highest temperature variation both in the grid-side and the machine-side MMC, and the situation in the grid-side MMC is worse than the machine-side MMC. It can also be seen that the highest junction temperature inside the MMC is around 110 °C, which is below the datasheet recommended temperature limit of 150 °C for the selected power switches. These temperature profile can be used to estimate the lifetime of the switches inside the MMC based on the lifetime model in 1 in section 2.2.1.

Table VI: The MMC parameters used for lifetime estimation

Parameters	Value	Unit
Power S	21	MVA
Number of submodules in each arm N_{SM}	8	/
Submodule voltage E_{SM}	3	kV
Submodule capacitance C_{SM}	20	mF
Submodule capacitor ESR R_{SM}	26.8	mΩ
Arm inductance L_{arm}	2.5	mH
Arm resistance R_{arm}	64.3	mΩ
PWM carrier frequency $f_{carrier}$	750	Hz
Powe switch type	Hitachi Energy	5SNA1000G650300



(a) Junction temperature variation in grid-side MMC, 5SNA1000G650300



(b) Junction temperature variation in machine-side MMC, 5SNA1000G650300

Fig. 17: Junction temperature variations with 5SNA1000G650300

4 Experiment results

4.1 Introduction to the experimental set-up

The experiment focuses on the waveform verification of the MMC converter, and the MMC experimental setup is shown in Fig 18.

Fig. 18: Lab set-up of the MMC: 1) DC power supply 2) MMC 3) Three-phase RL load

The set-up contains three main sections:

1. The DC power supply is from DELTA ELEKTRONIKA, and the model is SM 1500-CP-30. The supply voltage and current range of the DC power supply are $0 \sim 1500\,\mathrm{V}$ and $-30 \sim 30\,\mathrm{A}$ respectively. In the experiment setup, the DC power supply is used as a 400 V DC voltage source.
2. The five-level MMC cabinet is from Imperix power electronics. More details about the five-level MMC are described in 4.2.
3. The three-phase *RL* load, and the parameters are $R = 50\,\Omega$ and $L = 28\,\mathrm{mH}$. The three-phase load is being "star" connected.

4.2 Components of the five-level MMC

The inner part of the five-level MMC cabinet is shown in Fig. 19, and the MMC consists of 5 main parts, which can be divided into two main groups.

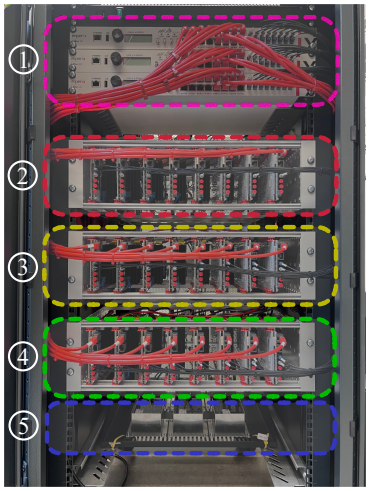


Fig. 19: Imperix converter cabinet: 1) Controllers 2)Phase A submodules 3) Phase B submodules 4) Phase C submodules 5) Arm inductors

The first group is the controller unit, and the model of the controller is called B-Box RCP. There are three controllers in total in the five-level MMC, and each controller contains 16 channels of PWM outputs. By feeding in the analog inputs to the controller, the PWM outputs can be generated at each sampling time, and in this way, the IGBT submodules are controlled. All the three BB-BOX RCP controllers are synchronized together to control the total 24 IGBT submodules in the five-level the MMC.

The second group is the electrical circuitry, and it contains 24 IGBT submodules and 6 arm inductors. The used IGBT submodule is shown in Fig. 20.

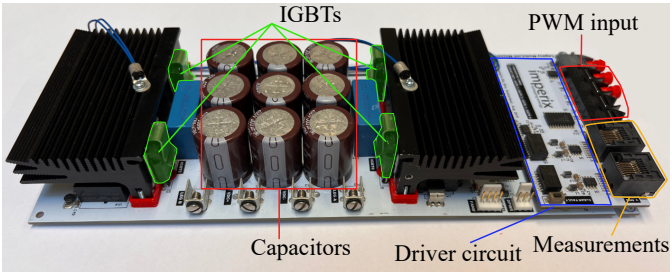


Fig. 20: The IGBT submodule inside the converter cabinet

The submodule includes 4× IGBT power switches on the board, forming a "H-bridge", while only two of the switches are used in the five-level MMC to form the half-bridge submodule. Apart from the power

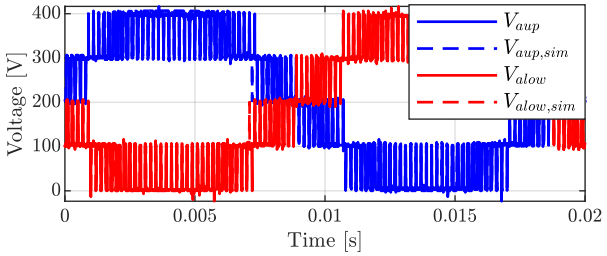
switches, the submodule also includes $9 \times PanasonicEET$ capacitors to form the submodule capacitor with a capacitance of 5 mF. The driver circuit, the optical PWM input, and the onboard measurements of the submodule are shown in Fig. 20 as well.

In addition to the IGBT submodules, there are 6 arm inductors in the electrical circuitry, which are placed at the bottom side of the converter cabinet, and the inductance is 2.3 mH for each arm.

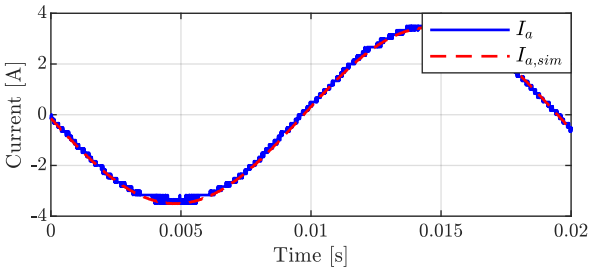
4.3 Experiment results of open-loop control

To demonstrate the working principle of the five-level MMC, an open-loop operation with using PWM modulation is firstly conducted.

The experiment and simulation results of the arm voltages and current of phase a of the five-level MMC with modulation index $m_a = 0.95$ are shown in Fig. 21. The switching frequency of each submodule is 5 kHz.



(a) Phase a up and low arm voltages



(b) Phase a current

Fig. 21: Phase a arm voltages and current, $m_a = 0.95$

In Fig. 21, it is shown that the experimental results are close to the simulation results, and for $m_a = 0.95$, all the four submodules in each arm are being operated.

The sampled submodule capacitor voltages ($f_{sampling} = 5\,\text{kHz}$) which are sent to the controller of phase a are shown in Fig. 22, and with the implemented sorting and balancing algorithm, all the 8 submodule capacitor voltages are balanced and controlled at the desired voltage level.

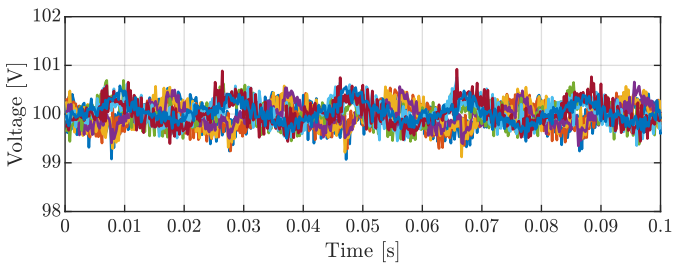


Fig. 22: Phase a submodule capacitor voltages

The arm currents and circulating current of phase a are shown in Fig. 23. The circulating current controller is activated at $t = 0.1$ s, and it can be seen that the oscillations of the circulating current are greatly suppressed with the aforementioned circulating current controller.

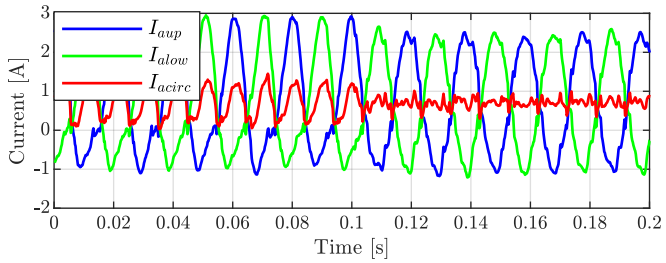


Fig. 23: Phase a arm currents and circulating currents

4.4 Experiment results of closed-loop control

The following sections show the experimental results when using the closed-loop current control for both the PWM and the SVM modulations. The closed-loop current controller is the classical PI controller which is implemented under dq coordinates. The DC-link voltage is set to be 400 V, which means each submodule is charged to 100 V. The nominal frequency of the system is set to be 50 Hz.

4.4.1 PWM modulation

Fig. 24 shows the experimental results when a d current step from 3.5 A to -1.5 A is activated at 0.5 s, and q current reference is set to be zero in the simulation.

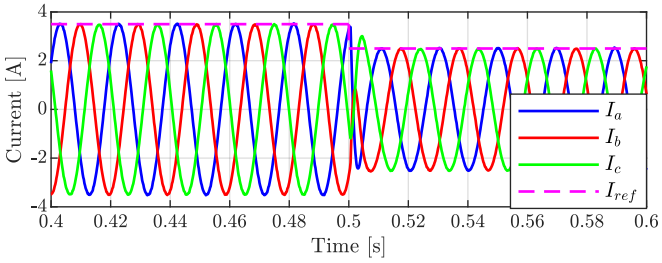
In Fig. 24a, the magenta curve is the amplitude of the reference current, and it can be seen that the amplitude of the three-phase currents can follow the reference value before and after the reference step. In addition to that, the current response is fast, and this is as expected since the bandwidth of the closed-loop current controller is designed as 1000 rad/s.

In Fig. 24b, the circulating current oscillations are minimized both before and after the current step. The DC component inside the circulating current decreases when the amplitude of the reference current is decreased, and this is as expected since the total delivered active power is decreased.

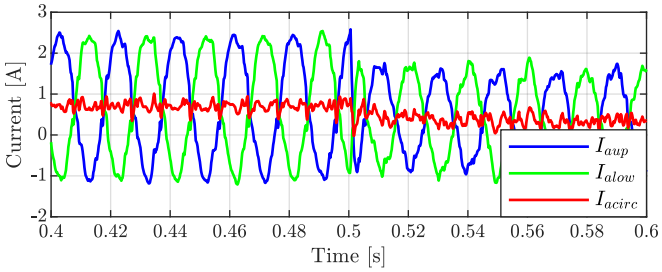
In Fig. 24c, the submodule voltages are balanced both before and after the current step. During the current step, the average submodule voltage is increased, and this is due to the higher oscillation inside the circulating current during the transient. Eventually, the average submodule voltage will go back to the reference value, which is 100 V.

4.4.2 SVM modulation

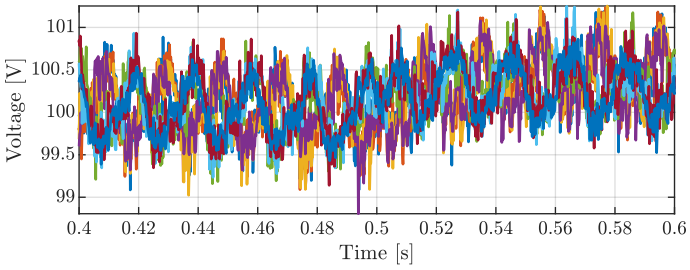
Figure. 25 shows the experimental results when the SVM modulation is implemented for the five-level MMC. As for the PWM modulation, it can be seen that for both of the current steps, the phase current amplitude can follow its reference value, the circulating currents are minimized, and the submodule capacitor voltages are balanced.



(a) Three-phase currents and current reference

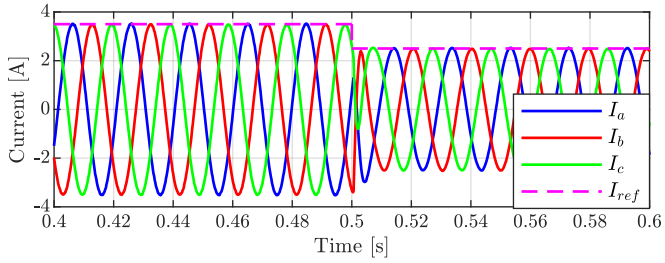


(b) Phase *a* arm and circulating currents

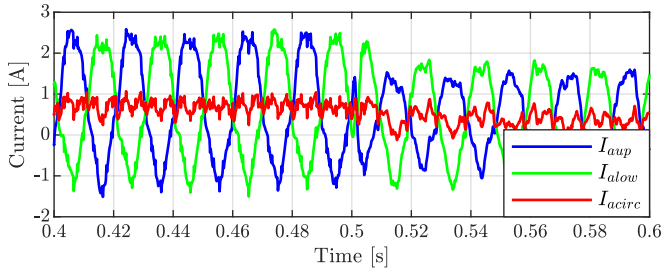


(c) Phase *a* submodule capacitors voltage

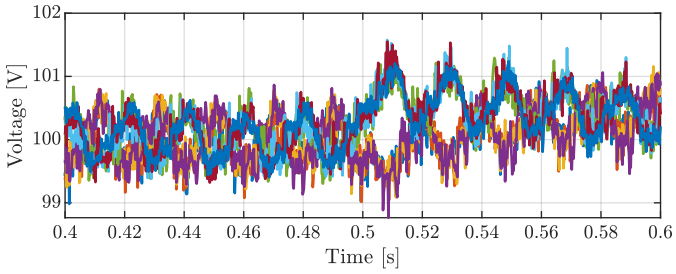
Fig. 24: Experimental results of PWM modulation with current step: 3.5 A to −2.5 A



(a) Three-phase currents and current reference



(b) Phase *a* arm and circulating currents



(c) Phase *a* submodule capacitors voltage

Fig. 25: Experimental results of SVM operation with current step: 3.5 A to -2.5 A

5 Conclusion

The present report documents the work that is done to fulfil the Deliverable 4.6, which is about the efficiency comparison between two-level converter and multi-level converter.

By using a comparative approach to simulate different converter topologies, it is shown that the nine-level MMC converter has the highest efficiency for the considered application. However, the nine-level MMC needs some extra investment due to the large amount of components. The second option is the five-level NPC, however, the uneven loss distribution of power switches and extra neutral point voltage control makes this topology less attractive. The third option is the five-level MMC, and the losses in the five-level MMC have the potential to be further decreased.

To sum up, the recommendation from this deliverable is to use the nine-level MMC for the defined application, and the key motivation is that the efficiency should have the highest priority.

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