PALMERA: Low Power and Fault Tolerant Cache Memory Design through Combined HW and SW Approaches

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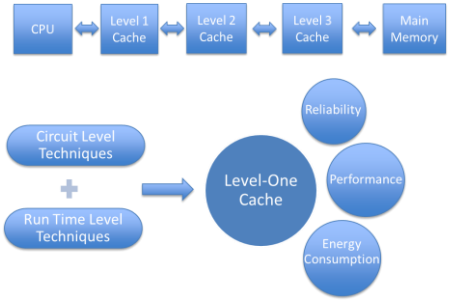
- Comprehensive study of applications and environments and get full information about their influence on the resilience of memories.
- Design and simulate novel cache memories which enables operation down to 320 mV and achieving up to one order of magnitude reduction in cache energy consumption under a given reliability constraint.
- Accompany run time level design methodologies to select the optimum operating mode and optimize energy consumption.
- Confirm the applicability of the proposed cache memory through evaluations using realistic industrial applications.



Outcomes

- Develop a cache memory and equip with novel circuit designs to keep the reliability during voltage scaling.
- Provide high capacity execution at nominal voltages and low energy and reliable execution at near threshold voltages.
- Proposed memory performs error detection/error correction action in one clock cycle.
- On top of circuit techniques, system scenario software techniques are used to select the optimum operating mode at run time.

Run Time Level Optimization

What happens while running in space:	Dynamically reconfigured according to the currently detected scenario
In runtime situations with high radiation:	Set to duplicate or triplicate data while still using nominal supply voltage, thus ensuring reliable operation.
With decreasing image resolution:	Set up with medium supply voltage, or even near-threshold supply voltage, thus saving additional energy.

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