Monday, 24.08.2015					
Room	Room 1	Room 2		Room 3	
08:45	Welcome Adresses				
09:00	Invited Talk: Professor Ronald Tetzlaff, Technische Universität Dresden				
10:00	Coffee				
10:30	Special: Counteracting Hardware Trojans with a Multidisciplinary Approach	**Circuit analysis**		**Memristive Circuits**	
		LNA Noise Parameter Measurement	Bernhard Lehmeyer, Michel T. Ivrlac and Josef A. Nossek	Memristor-Based Linear Feedback Shift Register Based on Material Implication Logic	Mehri Teimoory, Amirali Amirsoleimani, Arash Ahmadi, Shahpour Alirezaee, Saeideh Salimpour and Majid Ahmadi
		Novel Control Methods for Phase Lock Loops	Juergen Roeber, Christian Zwick, Andreas Baenisch, Simon Dirauf, Guenter Roppenecker and Robert Weigel	Memristive Crossbar Design and Test in Non-adaptive Proactive Reconfiguring Scheme	Peyman Pouyan, Esteve Amat and Antonio Rubio
		Finding All DC Solutions of Nonlinear Circuits Using Parallelogram LP Test	Kiyotaka Yamamura and Suguru Ishiguro	State transfer function and bandwidth limitation in a linear drift memristor model	Joakim Alvbrant, Vahid Keshmiri and J Jacob Wikner
		A Least Squares Method Applied to Multiphase Switched Capacitor Converters	Alexander Kushnerov and Alexandre Yakovlev	Memristor State-Space Embedding	Wael Dghais, Luis Nero Alves, Joana Catarina Mendes and José Carlos Pedro
		Complex Path Impedance Estimation and Matching Requirements for Body-Coupled Communication	Muhammad Irfan Kazim, Muhammad Imran Kazim and J Jacob Wikner	On the Usage of Harmonic Balance to Simulate Memristive Devices and Circuits	Rathnakannan Kailasam, Luis Nero Alves, Joana Catarina Mendes and José Carlos Pedro
12:10	Lunch				
13:10	Special: New Trends in the Theory and Applications of Cellular Nonlinear/ Nanoscale	**Communication Circuits**		**Computational Methods**	
		On 2D Reliability Schemes for Communications	Valeriu Beiu and Leonard Daus	Analog Layout Synthesis with Knowledge Mining	Po-Hsun Wu, Mark Po-Hung Lin and Tsung-Yi Ho
		A High Resolution and Low Jitter Linear Delay Line for IR-UWB Template Pulse Synchronization	Okan Zafer Batur, Naci Pekçokgüler, Günhan Dündar and Mutlu Koca	Pixel interlacing to trade off the resolution of a Cellular Processor Array against more registers	Julien Martel, Miguel Chau, Matthew Cook and Piotr Dudek

	Networks	Combined RF and multiphase PWM Transmitter	Muhammaf Fahim Ul Haque, Ted Johansson and Dake Liu	Statistical Analysis of Static Noise Margins	Valeriu Beiu and Mihai Tache
		Bandwidth-to-Area Comparison of Through Silicon Vias and Inductive Links for 3-D ICs	Ioannis Papistas and Vasilis Pavlidis	Realistic Path Loss Estimation for Capacitive Body-Coupled Communication	Muhammad Irfan Kazim, Muhammad Imran Kazim and J Jacob Wikner
		On Fixed-Point Implementation of\\Symmetric Matrix Inversion	Carl Ingemarsson and Oscar Gustafsson	Confidence Intervals at Multiconductor Transmission Lines with Stochastic Excitations	Lubomir Brancik and Edita Kolarova
14:50	Coffee Break & Poster Session				
19:00	Welcome Reception				

Tuesday, 25.08.2015					
	Room 1	Room 2		Room 3	
08:30	Invited Talk: dr. Scott Hanson, Ambiq Micro				
09:30	Coffee Break & Poster Session				
10:10	Special: System Scenarios for Designing Embedded and Photovoltaic Systems				
10:30		**Nonlinear Circuits**		**Oscillators**	
		Generalized Rule of Homothety of Ideal Memristors and Their Siblings	Zdenek Biolek, Dalibor Biolek, Viera Biolkova, Zdenek Kolka, Alon Ascoli and Ronald Tetzlaff	On Negative Resistance Oscillators as Modified Multi-vibrators	Erik Lindberg, K. Murali and Arunas Tamasevicius
		Remarks on the Adler's Equation	Antonio Buonomo and Alessandro Lo Schiavo	Phase noise spectrum of oscillators described by Ito stochastic differential equations	Michele Bonnin, Fernando Corinto, Fabrizio Bonani and Fabio Traversa
		Effective (Spur-Free) Dithering of Digital Delta-Sigma Modulators with Pseudorandom Dither	Hongjia Mo and Michael Peter Kennedy	Linearization of Synthesizable VCO-Based ADCs Using Delta Modulation	Vishnu Unnikrishnan and Mark Vesterbacka
		A Complete Classification of Memristor Devices	Fernando Corinto, Pier Paolo Civalleri and Leon Chua	A Differential Inverter-based Switched-Capacitor Oscillator in 65 nm CMOS Technology	Peng Wang, Gyorgy Csaba, Wolfgang Porod and Trond Ytterdal

		Complex behavior in memristor circuit based on static nonlinear two-ports and dynamic bipole	Jacopo Secco, Mario Biey, Fernando Corinto, Alon Ascoli and Ronald Tetzlaff	A micro power temperature compensated frequency generating circuit	Shailesh Singh Chouhan and Kari Halonen
12:10	Lunch				
13:10	Special: Asynchronous Circuits	**Filters and methods**		**Neuromorphic & Biomedical Circuits**	
		Narrowest Band-pass Digital FIR Filters	Pavel Zahradnik, Miroslav Vlcek, Michal Susta and Boris Simak	A high dynamic range image sensor with linear response based on asynchronous event detection	Juan A. Leñero-Bardallo, Ricardo Carmona-Galán and Ángel Rodríguez-Vázquez
		PVT Variations in Differential Flip-Flops: A Comparative Analysis	Massimo Alioto, Gaetano Palumbo and Elio Consoli	Negative Resistance Circuit for Damping an Array of Coupled FitzHugh-Nagumo Oscillators	Arunas Tamasevicius, Elena Adomaitiene, Skaidra Bumeliene, Gytis Mykolaitis and Erik Lindberg
		Relationships Between Two Definitions of Fading Memory for Discrete-Time Systems	Andrzej Borys	Inductive Charging of an EDLC Powered Wristband Device for Medical Measurements	Stijn Wielandt, Bart Thoen, Jean-Pierre Goemaere, Lieven De Strycker and Nobby Stevens
		Voltage-Mode All-Pass Filter Passive Scheme Based on Floating Negative Resistor and Grounded Capacitor	Norbert Herencsar, Jaroslav Koton, Kamil Vrba, Shahram Minaei and İzzet Cem Göknar	Inverter-based Low-power, Low-noise SC-VGA and 8 Channel Pipelined S/H Analog Beamformer for Ultrasound Imaging Probes	Peng Wang and Trond Ytterdal
		Design Approach for a Class of 2D Recursive Filters	Radu Matei	Power-Efficient Estimation of Silicon Neuron Firing Rates with Floating-Gate Transistors	Stephen Nease and Elisabetta Chicca
		Design of Current-Mode Class 1 Frequency-Agile Filter Employing CDTAs	Mesut Atasoyu, Hakan Kuntman, Bilgin Metin, Norbert Herencsar and Oguzhan Cicekoglu		
15:10	Coffee Break				
15:40	Award Ceremony (Best Student Paper Award) / Invitation to ECCTD 2017				
19:00	Conference Dinner				

Wednesday, 26.08.2015

	Room 1	Room 2		Room 3	
08:30	Invited Talk: Professor Wolfgang Kunz, Technische Universität Kaiserslautern, Germany Hardware/Firmware Verification in System-Level Design Flows – Can Formal Methods Meet the Challenge?				
09:30	Coffee Break				
10:00	Special: Design of Smart Integrated Energy-Harvesting Systems	**Converters**		**Analog Circuit Design**	
		A Fully-Differential OTA in 28 nm UTBB FDSOI CMOS for PGA Applications	Prakash Harikumar, J Jacob Wikner and Atila Alvandpour	A High Voltage Current Sense Amplifier With Extended Input Common Mode Range Based On A Low Voltage Operational Amplifier Cell	Razvan Puscasu, Pavel Brinzoi, Laurentiu Creosteanu and Gheorghe Brezeanu
		A Digitally Assisted 20MHz-600MHz 16-Phase DLL Enhanced with Dynamic Gain Control Loop	Arash Hejazi, Sarang Kazeminia and Roozbeh Abdollahi	Design of an Op-Amp Free Voltage Reference with PWM Regulation	Pinar Basak Basyurt, Edoardo Bonizzoni, Franco Maloberti and Devrim Yilmaz Aksin
		Low Power Continuous-Time Delta-Sigma ADC with Current Output DAC	Niels Marker-Villumsen, Ivan H. H. Jørgensen and Erik Bruun	Design of Current Mode Front-end Amplifiers with Optimal Timing Performance for High-gain Photodetectors	Fabio Ciciriello, Francesco Corsi, Francesco Licciulli, Cristoforo Marzocca and Gianvito Matarrese
		A High Resolution Time-to-Digital Converter Utilizing Coupled Oscillator, ORIGAMI	Takeshi Shima and Nicodimus Retdian	New Sensor Concept for Intra-Frame Scene and Speed Capturing	Máté Németh and Ákos Zarándy
		A digitally corrected bandgap voltage reference with a 3σ temperature coefficient of 3.8 ppm/K	Hannes Badertscher, Armin Stocklin, Roman Willi, Andreas Fitzi and Paul Zbinden	Single-Miller All-Passive Compensation Network for Three-Stage OTAs	Giuseppe Di Cataldo, Alfio Dario Grasso, Gaetano Palumbo and Salvatore Pennisi
		The Synthesis of Noise Transfer Functions for Bandpass Delta-Sigma Modulators with Tunable Center Frequency	Enrico Roverato, Marko Kosunen and Jussi Ryynänen	VLSI Hybrid DC-DC Regulator	Jordi Cosp-Vilella and Herminio Martinez-Garcia
12:00	Lunch				

		RF		Semiconductor Devices and Technology	
13:00	Special: Power Converters for Energy Harvesting	Clock Phase Imbalance and Phase Noise in RF N-path Filters	Fahad Qazi and Jerzy Dabrowski	Exploiting Short Channel Effects and Multi-Vt Technology for Increased Robustness and Reduced Energy Consumption, with application to a 16-bit Subthreshold Adder Implemented in 65 nm CMOS	Ali Asghar Vatanjou, Trond Ytterdal and Snorre Aunet
		Generation of parameterized macromodels of two-port RF circuits for SPICE simulator	Katarzyna Opalska	A Fully Integrated Audio Amplifier in Flexible a-IGZO TFT Technology for Printed Piezoelectric Loudspeakers	Reza Shabanpour, Corrado Carta, Tilo Meister, Koichi Ishida, Bahman Kheradmand-Boroujeni, Niko Stephan Munzenrieder, Giovanni Antonio Salvatore, Luisa Petti, Gerhard Troester and Frank Ellinger
		Reduction of Harmonic Balance Equations Through Galerkin's Method	Federico Bizzarri, Angelo Brambilla and Lorenzo Codecasa	Impact of Guard Ring Layout on the Stacked Low-Voltage PMOS for High-Voltage ESD Protection	Seian-Feng Liao, Kai-Neng Tang, Ming-Dou Ker, Jia-Rong Yeh, Hwa-Chyi Chiou, Yeh-Jen Huang, Chun-Chien Tsai, Yeh-Ning Jou and Geeng-Lih Lin
		All-Digital Phase-Locked Loop in 40 nm CMOS for 5.8 Gbps Serial Link Transmitter	Yury Antonov, Tero Tikka, Kari Stadius and Jussi Ryynänen	Compensation Circuit with Additional Junction Sensor to Enhance Latchup Immunity for CMOS Integrated Circuits	Hui-Wen Tsai and Ming-Dou Ker
		An Improved Estimation Method of 4 port S-parameters with 2 port Measurements	Noboru Maeda, Shinji Fukui, Toshikazu Sekine and Yasuhiro Takahashi	A 65 nm Standard Cell Library for Ultra Low-power Applications	Marten Vohrmann, Saikat Chatterjee, Sven Lütkemeier, Thorsten Jungeblut, Mario Porrmann and Ulrich Rückert
14:40	Conference end				